LISTING OF CLAIMS:

1. (Original) A circuit for activating a test mode of a semiconductor memory device, comprising:

a test mode controller means for outputting a test mode setting signal to control a test mode setting operation in response to a mode register set signal and an address signal;

a test mode decoder means, controlled by the test mode setting signal, for selecting a test mode item group among a plurality of test mode item groups in response to upper address bits of the address signal; and

a test mode item selecting means for selecting a predetermined test mode item out of the test mode item group selected by the test mode decoder means in response to lower address bits of the address signal,

wherein the test mode item group comprises a predetermined number of test mode items among a plurality of test mode items.

2. (Currently Amended) The circuit according to claim 1, wherein ~~the test mode decoder means is controlled by the test mode setting signal and~~ the test mode decoder means comprises a plurality of group selecting means for outputting a plurality of group selecting signals in response to upper address bits of the address signal,

wherein each of the plurality of group selecting signals ~~signal~~ is a signal to select a predetermined test mode item group among the plurality of test mode item groups.

3. (Original) The circuit according to claim 2, wherein each of the group selecting means comprises:

a pull-up means for pulling up an output terminal in response to a first signal outputted from the test mode controller means; and

a first pull-down means for pulling down the output terminal in response to the corresponding upper address bits.

4. (Original) The circuit according to claim 3, wherein each of the group selecting means is connected between the output terminal and the first pull-down means and further comprises a second pull-down means for pulling down the output terminal in response to a second signal outputted from the test mode controller means.

5. (Original) The circuit according to one of claims 3 and 4, wherein each group selecting means further comprises a latch means for maintaining a potential of the output terminal.

6. (Original) The circuit according to claim 1, wherein the test mode item selecting means comprises a plurality of item selecting means for selecting a corresponding test mode item out of the test mode item group selected by an output signal from the test mode decoder means in response to the lower address bits.

7. (Original) The circuit according to claim 1, further comprising a first address decoder means for decoding the upper address bits and outputting a first decoded address signal to the test mode decoder means.

8. (Original) The circuit according to one of claims 1 and 7, further comprising a second address decoder means for decoding the lower address bits and outputting a second decoded address signal to the test mode item selecting means.

9. (Original) A circuit for activating a test mode of a semiconductor memory device, comprising:

a test mode controller circuit configured to output a test mode setting signal suitable for controlling a test mode setting operation in response to a mode register set signal and an address signal;

a test mode group decoder circuit configured to receive the test mode setting signal and upper address bits of the address signal and, in response thereto, output a test mode group signal indicating a test mode item group selected from among a plurality of test mode item groups; and

a test mode selecting circuit configured to receive lower address bits of the address signal and the test mode group signal and, in response thereto, output a test mode item signal indicating a selected test mode to be performed,

wherein the test mode item group comprises a predetermined number of test modes among a plurality of test modes.

10. (Currently Amended) The circuit according to claim 9, wherein the test mode group decoder circuit receives the test mode setting signal and further comprises a plurality of group selecting circuits configured to receive upper address bits of the address signal and output a plurality of group selecting signals in response thereto,

wherein each of the plurality of group selecting signals ~~signal~~ is a signal indicating selection of a predetermined test mode item group from among the plurality of test mode item groups.

11. (Original) The circuit according to claim 10, wherein each of the plurality of group selecting circuits further comprises:

a pull-up circuit coupled to an output terminal and the test mode controller circuit and configured to pull up a voltage on the output terminal in response to a first signal received from the test mode controller circuit; and

a first pull-down circuit configured to receive the upper address bits and pull down the voltage on the output terminal in response thereto.

12. (Original) The circuit according to claim 11, wherein each of the plurality of group selecting circuits is connected between the output terminal and the

first pull-down circuit and further comprises a second pull-down circuit coupled to the output terminal and the test mode controller circuit and configured to pull down the voltage on the output terminal in response to a second signal received from the test mode controller circuit.

13. (Original) The circuit according to claim 11, wherein each of the plurality of group selecting circuits further comprises a latch circuit configured to maintain a voltage potential of the output terminal.

14. (Original) The circuit according to claim 9, wherein the test item selecting circuit comprises a plurality of mode selecting circuits each coupled to the test mode group decoder circuit and configured to receive the lower address bits and output a particular test mode signal in response to an output signal received from the test mode group decoder circuit and the lower address bits.

15. (Original) The circuit according to claim 9, further comprising a first address decoder circuit configured to receive the upper address bits and, in response thereto, output a first decoded address signal to the test mode group decoder circuit.

16. (Original) The circuit according to claim 15, further comprising a second address decoder circuit configured to receive the lower address bits and, in response thereto, outputting a second decoded address signal to the test mode selecting circuit.